



PTO/SB/08a (08-03)

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use as many sheets as necessary)		Application Number	10/736,908		
		Filing Date	12/17/2003		
		First Named Inventor	Frederic Josso et al.		
		Art Unit	2123 2825		
		Examiner Name	JBD S. WHITMORE		
Sheet	1	of	2	Attorney Docket Number	003921.00137

U.S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number - Kind Code ² (if known)			
JW		US- 4,860,290	08-22-1989	Daniels et al.	
		US- 5,036,473	07-30-1991	Butts et al.	
		US- 5,109,353	04-28-1992	Sample et al.	
		US- 5,572,710	11-05-1996	Asano et al.	
		US- 5,596,742	01-21-1997	Agarwal et al.	
		US- 5,777,489	07-07-1998	Barbier et al.	
		US- 5,821,773	10-13-1998	Norman et al.	
		US- 5,870,586	02-09-1999	Baxter	
		US- 5,943,490	08-24-1999	Sample	
		US- 6,002,861	12-14-1999	Butts et al.	
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		US- 6,265,894 B1	07-24-2001	Reblewski et al.	
		US- 6,282,503	08-28-2001	Okazaki et al.	
		US- 6,377,912 B1	04-23-2002	Sample et al.	
		US- 6,388,465	05-14-2002	Barbier et al.	
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		US- 6,625,793 B2	09-23-2003	Sample et al.	
		US- 6,694,464 B1	02-17-2004	Quayle	
		US- Re. 34,363	08-31-1993	Freeman, deceased	

FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³ - Number ⁴ - Kind Code ⁵ (if known)				
JW		EP 0,651,343 A1	05-03-1995	Quickturn Systems Inc.		
JW		WO 94/06210	03-17-1994	Goell, Prabhakar		

Examiner Signature		Date Considered	3/29/07
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Sheet	2	of	2	Attorney Docket Number	003921.00137

NON PATENT LITERATURE DOCUMENTS			
Examiner Initials *	Cite No. 1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T 2
AW		Erhard et al., W. First Steps Towards a Reconfigurable Asynchronous System, IEEE International Workshop on Rapid System Prototyping, 1999, pgs. 28-31	
AW		Kocan et al., F. Concurrent D-Algorithm on Reconfigurable Hardware, IEEE/ACM International Conference on Computer-Aided Design, 1999, Digest of Technical Papers, pgs. 152-155	
		Clos, Charles, "A study of Non-Blocking Switching Networks," The Bell System Technical Journal, March 1953, pgs. 408-424	
		Bosi et al., B. Reconfigurable Pipelined 2-D Convolvers for Fast Digital Signal Processing, IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 7, Issue 3, Sept. 1999, pgs. 299-308	
		Ejnoui et al., A. Design Partitioning on Single-Chip Emulation Systems, 13 th International Conference on VLSI Design, 2000, pgs. 234-239	
		Jean, J.S.N., et al., "Dynamic Reconfiguration to Support Concurrent Applications," IEEE Transactions on Computers, June 1999, IEEE, USA, vol. 48, No. 6, pgs. 591-602	
		Snider, G., "The Teramac Compiler," Nov. 29, 1993, pgs. 1-51	
		Xilinx, "The Programmable Gate Array Design Handbook", First Edition, 1986, pgs. i-A10	
		Babb, J, et al., "Logic Emulation with Virtual Wires," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, June 1997, pgs. 1-20	

Examiner Signature	<i>Ng hte</i>	Date Considered	3/29/07
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